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QUESTA INSPECT

Improve design quality without a testbench with deep sequential analysis

Questa Inspect provides a powerful formal verification tool that automatically identifies and addresses challenging sequential issues in RTL designs without the need for a testbench. By executing push-button RTL assertion synthesis, Questa Inspect offers a bottom-up verification process that significantly improves design quality and detects bugs that traditional simulation may miss.

With an intuitive interface and automated checks for initialization, functional, and coverage issues, Questa Inspect seamlessly integrates into your development process, enhancing verification accuracy and streamlining debugging.

Why Choose Questa Inspect for Formal Verification?

Deep sequential analysis without a testbench

Questa Inspect performs comprehensive formal verification of complex sequential logic issues, eliminating the need for time-consuming testbench creation. This speeds up the verification process while identifying bugs that traditional methods may overlook.

Automated formal checks

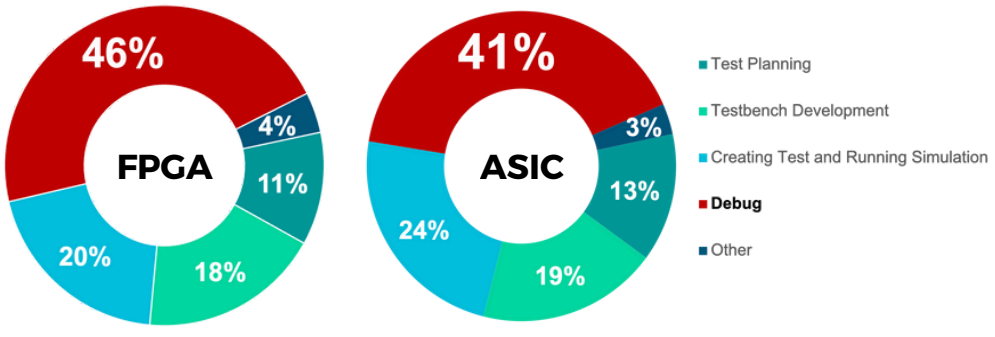
Questa Inspect automates key design rule checks, including initialization, functional issues, and coverage reachability. These checks are automatically synthesized into assertions, simplifying the verification process and improving accuracy without manual effort.

User-friendly debugging environment

With dedicated GUI windows for debugging, Questa Inspect provides focused structural debug tools. Designers can visualize issues in real-time with intuitive schematic, waveform, and source code views, ensuring faster issue resolution.

Integration into existing workflows

Questa Inspect easily integrates with RTL design environments and continuous integration flows, supporting both ASIC and FPGA designs. Its mixed-language support for Verilog, SystemVerilog, and VHDL makes it flexible for various development processes.

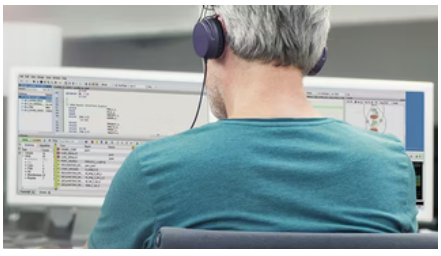


The chart clearly highlights that **debugging** is the largest verification time consumer, occupying 46% for FPGA and 41% for ASIC projects. This significant share emphasizes the importance of efficient debugging tools like **Questa Inspect**, which can drastically reduce the time spent in this phase. By automating and streamlining the debug process, teams can shift focus toward other critical tasks, such as testbench development and test planning, improving overall productivity.

Key Features of Questa Inspect

Sequential Analysis

Questa Inspect identifies deep sequential issues in designs that are often difficult to trigger and detect using traditional simulation. This ensures that even complex bugs are found early in the design process.



Automated Formal Checks

Questa Inspect automates formal checks to identify issues like uninitialized registers, X propagation, combinational loops, FSM errors, and unreachable logic. This ensures comprehensive verification and robust coverage reachability without manual intervention.

Focused Debugging Environment

Questa Inspect provides a comprehensive GUI with debugging windows for checks, waveforms, source code, and FSM details. Automatically generated reports streamline the debugging process, allowing users to quickly pinpoint and resolve issues.

Push-button Verification

With its push-button approach, Questa Inspect allows users to perform in-depth verification without writing properties or creating testbenches. The automatic generation of assertions reduces manual intervention, allowing designers to focus on critical design issues.

Integration and Usability

Questa Inspect seamlessly integrates into existing design flows, supporting mixed-language environments (Verilog, SystemVerilog, VHDL) and working with both RTL and netlist designs. It is compatible with continuous integration environments, making it ideal for both ASIC and FPGA verification.