

QUESTA EQUIVALENT FPGA

Advanced equivalence checking for reliable FPGA implementation and optimization

Questa Equivalent FPGA ensures design integrity throughout the FPGA implementation flow, supporting advanced architectures and optimizations like DSP inference, FSM re-encoding, and register pipelining. It accelerates verification, reduces gate-level simulations, and detects difficult-to-find implementation flow issues early.

With tailored support for FPGA vendor tools and device-specific optimizations, Questa Equivalent FPGA provides unmatched accuracy in pinpointing design discrepancies, ensuring that your design functions as intended throughout all stages of synthesis and place-and-route (P&R).

Why Choose Questa Equivalent FPGA?

Improved functionality, performance, and cost

Questa Equivalent FPGA enhances the quality of FPGA designs by enabling advanced verification methods across modern FPGA architectures. It helps reduce verification time and ensure functional correctness even after complex synthesis and P&R optimizations.

Comprehensive RTL verification across FPGA implementation

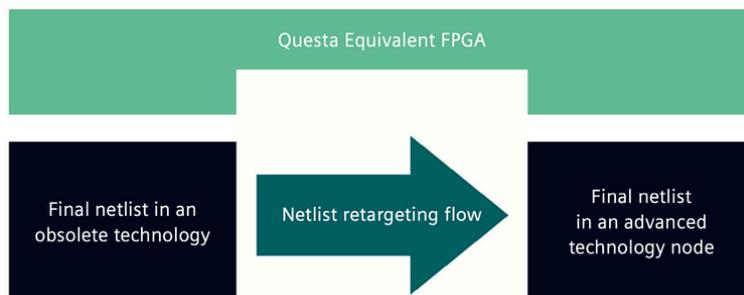
Questa Equivalent FPGA ensures equivalence from RTL to the final netlist, combining powerful combinational and sequential provers. It addresses FPGA-specific challenges, such as register pipelining and FSM re-encoding, guaranteeing consistency throughout the implementation.

Faster error detection and debugging

With Questa Equivalent FPGA, you can rapidly verify modern FPGA optimization flows and pinpoint the exact source of implementation errors, significantly reducing debug cycles. This speeds up the design process and minimizes gate-level simulations.

Integration with vendor-specific tools

Questa Equivalent FPGA directly integrates with leading FPGA vendor tools, including AMD-Xilinx Vivado, Intel Quartus, and Microchip Libero, ensuring a smooth setup and verification process with automated script generation and seamless mapping to the chosen FPGA technology.



The Questa Equivalent FPGA retargeting flow helps extend the lifespan of legacy designs while leveraging the latest FPGA advancements in performance, power efficiency, and safety features.

Key Features of Questa Equivalent FPGA



Advanced FPGA Implementation Verification

Questa Equivalent FPGA provides exhaustive verification coverage for modern FPGA designs, supporting advanced optimizations like DSP inference, FSM re-encoding, and RAM/ROM inference. By verifying the implementation flow, it ensures that your design maintains functional equivalence from RTL to the final netlist.



Combinational and Sequential Provers

Combining advanced combinational and sequential provers, Questa Equivalent FPGA tackles complex FPGA-specific issues, such as register pipelining, retiming, and clock domain crossings. This allows for a thorough verification process, ensuring that optimizations do not introduce functional discrepancies.



Rapid Error Detection and Debugging

With powerful debugging tools, Questa Equivalent FPGA quickly identifies and isolates design issues, providing focused counterexample resolution. The tool's GUI visualization, auto-reset detection, and trace generation accelerate the process of finding and fixing errors, reducing verification bottlenecks.



Device-Specific Optimization Support

Questa Equivalent FPGA integrates seamlessly with leading FPGA vendor tools such as AMD-Xilinx Vivado, Intel Quartus, and Microchip Libero, offering device-specific profiling. It supports advanced architectural features, enabling efficient verification for optimizations like register packing, retiming, and power optimization.



Minimized Gate-Level Simulation

Questa Equivalent FPGA reduces the need for time-consuming gate-level simulations by providing formal equivalence checking, making it easier to verify FPGA designs without compromising quality or increasing verification time. This significantly shortens the overall design and verification cycle.